CLAIMS

What is claimed is:

1. A method of fabricating a metal-oxide semiconductor (MOS) transistor with low gate depletion and high gate drivability in nitride read only memory (NROM), the method comprising:

providing a semiconductor wafer with a memory array area and a peripheral circuit region defined on a surface of a substrate of the semiconductor wafer;

forming a silicon oxide layer on a surface of the peripheral circuit region;

forming an amorphous silicon layer on a surface of the silicon oxide layer;

forming a silicon germanium layer on a surface of the amorphous silicon layer;

patterning the silicon germanium layer and the amorphous silicon layer to form a gate of the MOS transistor on the surface of the substrate;

forming a spacer around the gate;

forming a source and a drain of the MOS transistor in the substrate;

forming a nickel (Ni) layer on a top surface of the gate; and

performing a rapid thermal annealing process (RTA process) for reacting the nickel layer with the silicon germanium layer on the top surface of the gate, forming a silicon nickel layer.

2. The method of claim 1 wherein the substrate is a silicon substrate.

3. The method of claim 1 wherein the chemical composition of

the silicon germanium layer is $Si_{1-x}Ge_x$, x = 0.05~1.0.

4. The method of claim 1 wherein patterning the silicon germanium layer further patterning the silicon oxide layer.

5. The method of claim 1 wherein the silicon oxide layer functions as a gate oxide layer of the MOS transistor, and the amorphous silicon layer, the silicon germanium layer and the silicon nickel layer function as a gate conductive layer of the MOS transistor.

6. The method of claim 1 wherein the MOS transistor is an NMOS transistor or a PMOS transistor.

7. The method of claim 1 further comprising performing a first ion implantation process for forming a lightly doped drain (LDD) of the MOS transistor.

8. The method of claim 1 wherein the method of forming the source and drain comprises:

performing a second ion implantation process to form two doped areas on the substrate on two sides of the gate; and

performing a thermal annealing process to drive dopants into the two doped areas for forming the source and drain.

9. The method of claim 8 wherein the thermal annealing process diffuses germanium atoms of the silicon germanium layer into the amorphous silicon layer, transforming the amorphous silicon layer into silicon germanium.

10. The method of claim 1 wherein the silicon germanium layer

is formed by performing a chemical vapor deposition (CVD) process aerating silane (SiH_4), germane (GeH_4), and hydrogen at a temperature ranging between 450°C and 620°C.

11. The method of claim 1 wherein the memory array area is used to form a plurality of NROM memory cells and each NROM memory cell comprises a MOS transistor and a silicon nitride layer.

12. A method of fabricating a metal-oxide semiconductor (MOS) transistor with low gate depletion and high gate drivability, the method comprising:

providing a semiconductor wafer;

forming a silicon oxide layer on a surface of the silicon substrate of the semiconductor wafer;

performing an in-situ doped chemical vapor deposition (CVD) process for forming a silicon germanium layer on a surface of the silicon oxide layer;

patterning the silicon germanium layer to form a gate of the MOS transistor on the surface of the silicon substrate;

forming a spacer around the gate;

performing a first ion implantation process to form two doped areas on the silicon substrate on two sides of the gate;

performing a thermal annealing process to drive dopants into the two doped areas, thereby forming a source and a drain of the MOS transistor;

forming a nickel (Ni) layer on a top surface of the gate; and

performing a rapid thermal annealing process (RTA process) for reacting the nickel layer with the silicon germanium layer on the top surface of the gate, forming a silicon

nickel layer.

13. The method of claim 12 wherein patterning the silicon germanium layer further patterning the silicon oxide layer.

14. The method of claim 12 wherein the silicon oxide layer functions as a gate oxide layer of the MOS transistor, and the silicon germanium layer and the silicon nickel layer function as a gate conductive layer of the MOS transistor.

15. The method of claim 12 wherein the MOS transistor is an NMOS transistor or a PMOS transistor.

16. The method of claim 12 further comprising a second ion implantation process for forming a lightly doped drain (LDD) of the MOS transistor.

17. The method of claim 12 wherein the process gases of the in-situ doped CVD process comprise silane (SiH_4), germane (GeH_4) and hydrogen, and temperature of the in-situ doped CVD process ranges between 450℃ and 620℃.